WHAT IS CLAIMED IS:

1. A method for verifying scan chain equivalency between two representations of a circuit design having at least one scannable state element, at least one scan-out and at least one output pin, comprising:

for each representation of the circuit design, loading each scannable state element with a symbolic expression that characterizes a logical location of said scannable element in the circuit design; and

for each representation of the circuit design, performing a scan shift operation to verify the contents of each scannable state-element at said scan-out and output pins of the design.

2. The method of claim 1, wherein the two representations of a circuit design comprise a switch-level netlist and an RTL netlist.

3. The method of claim 1, wherein the two representations of a circuit design comprise a transistor level implementation and a behavioral level description.

4. The method of claim 1, wherein the two representations of a circuit design comprise RTL and schematic models of a memory circuit.

5. The method of claim 1, wherein the two representations of a circuit design comprise a first RTL model of a storage circuit and a second RTL model of a storage circuit.

6. The method of claim 1, wherein the two representations of a circuit design comprise a SPICE-level netlist and a gate level description.

7. The method of claim 1, wherein said loading of each scannable state element with a symbolic expression comprises simulating said circuit design in a functional mode for a

first minimum threshold number of cycles by applying symbolic expressions to at least a first input for said circuit design.

8. The method of claim 7, wherein said first minimum threshold number comprises the maximum sequential depth of all scannable state-elements on all paths from all primary inputs in said circuit design.

9. The method of claim 1, wherein said loading and performing steps are implemented with a symbolic simulator to check scan chain equivalency with respect to complete scan chain connectivity from primary input to primary output, logical location of all scannable state elements, scan chain length and scan chain order.

10. The method of claim 1, wherein said loading and performing steps are implemented with a symbolic simulator to obtain complete coverage.

11. The method of claim 1, wherein said scan shift operation comprises simulating a sequence of scan clocks equal to a multiple of the number of scannable state-elements in the circuit design.

12. An article of manufacture having at least one recordable medium having stored thereon executable instructions and data which, when executed by at least one processing device, cause the at least one processing device to verify equivalency of a scan chain design comprising at least a first scannable memory-element by:

storing a first representation of a scan chain design;

storing a second representation of the scan chain design;

symbolically simulating the scan chain design by applying symbolic inputs to inputs in the first and second representations of the scan chain design;

performing a scan shift on the first and second representations to verify the contents of each scannable memory element at an output of the scan chain design.

13. The article of manufacture defined in claim 12, wherein the instructions and data cause the at least one processing device to symbolically simulate the scan chain design by loading each scannable memory element in the scan chain design with a symbolic expression that is characteristic of a logical location for that scannable memory element.

14. The article of manufacture defined in claim 12, wherein the first representation comprises an RTL level description of the scan chain design, and the second representation comprises an schematic level description of the scan chain design.

15. The article of manufacture defined in claim 12, wherein the instructions and data cause the at least one processing device to symbolically simulate the scan chain design by symbolically simulating the scan chain design in functional mode for a threshold number of cycles, where the threshold number equals the maximum of all sequential depths of all scannable memory elements on all paths from all primary inputs in the scan chain design.

16. The article of manufacture defined in claim 15, wherein the instructions and data cause the at least one processing device to perform scan shifting after the scan chain design has been symbolically simulated in function mode to thereby verify the contents of each scannable memory element at a scan-out pin of the design.

17. The article of manufacture defined in claim 12, wherein the scan chain design comprises at least a portion of microprocessor circuitry.

18. The article of manufacture defined in claim 12, wherein the scannable memory element comprises a flop-flop.

19. A scan chain integrated circuit, comprising:

a plurality of circuit components for processing data signals in accordance with a timing sequence controlled by at least one clock signal; and

one or more scannable state-elements for use in performing DFT testing on the plurality of circuit components;

wherein the design of said scan chain integrated circuit is verified by:

(a) generating a first description of the scan chain integrated circuit comprising a representation at a first level of abstraction;

(b) generating a second description of the scan chain integrated circuit comprising a representation at a second level of abstraction;

(c) loading each scannable state-element in the first and second descriptions with a unique symbol characterizing the logical location of the scannable state-element in the scan chain integrated circuit design;

(d) symbolically simulating the first and second descriptions in functional mode; and

(e) performing a scan shift on the first and second descriptions to verify equivalency of the first and second descriptions by checking the contents of said scannable state-element at a first and second output of said first and second descriptions.

20. The scan chain integrated circuit of claim 19, wherein the first description comprises a switch-level netlist description, and the second description comprises an RTL netlist.